1. Description

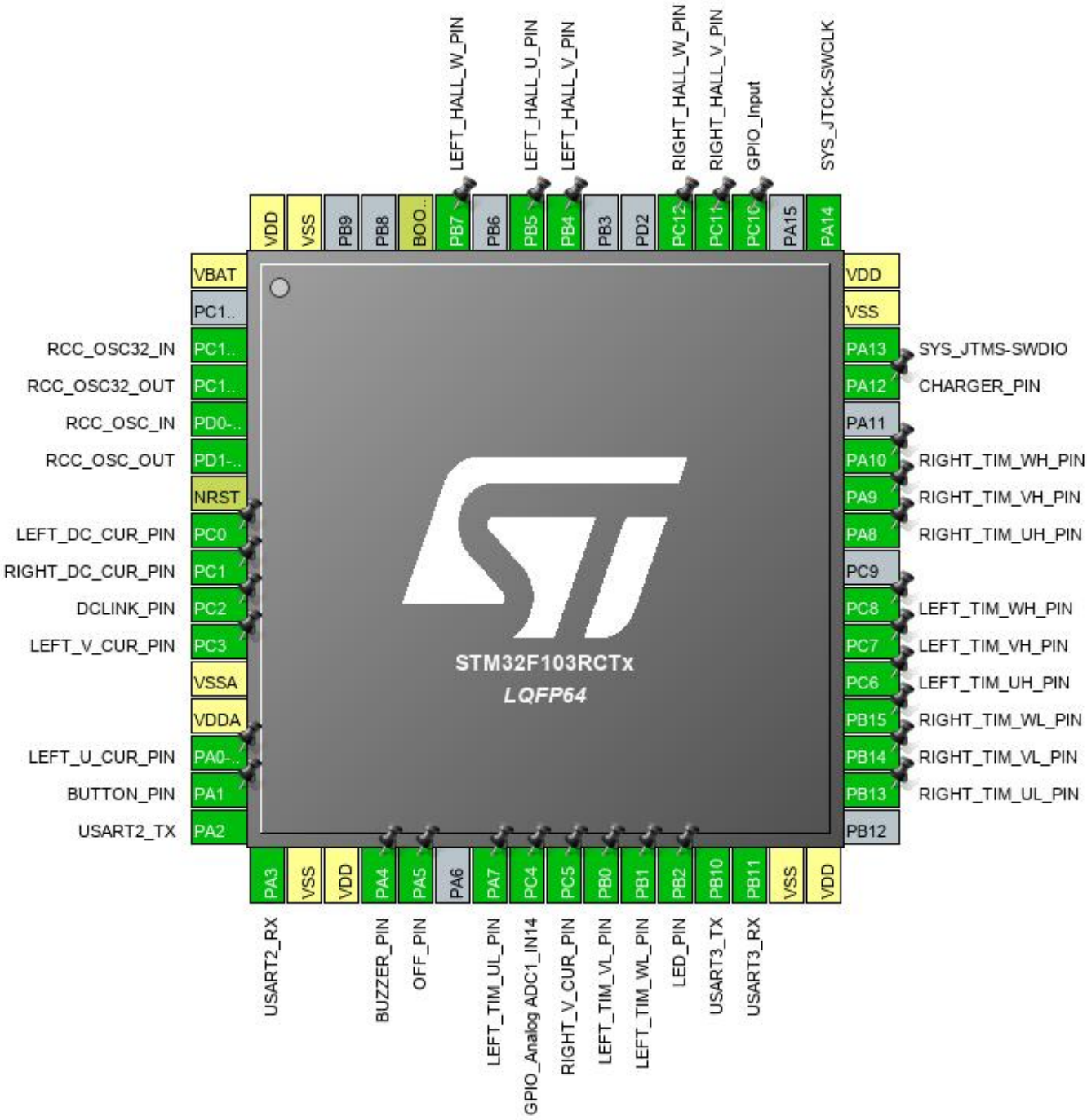
1.1. Project

Project Name	SideBoardMX
Board Name	custom
Generated with:	STM32CubeMX 5.1.0
Date	06/19/2019

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RCTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



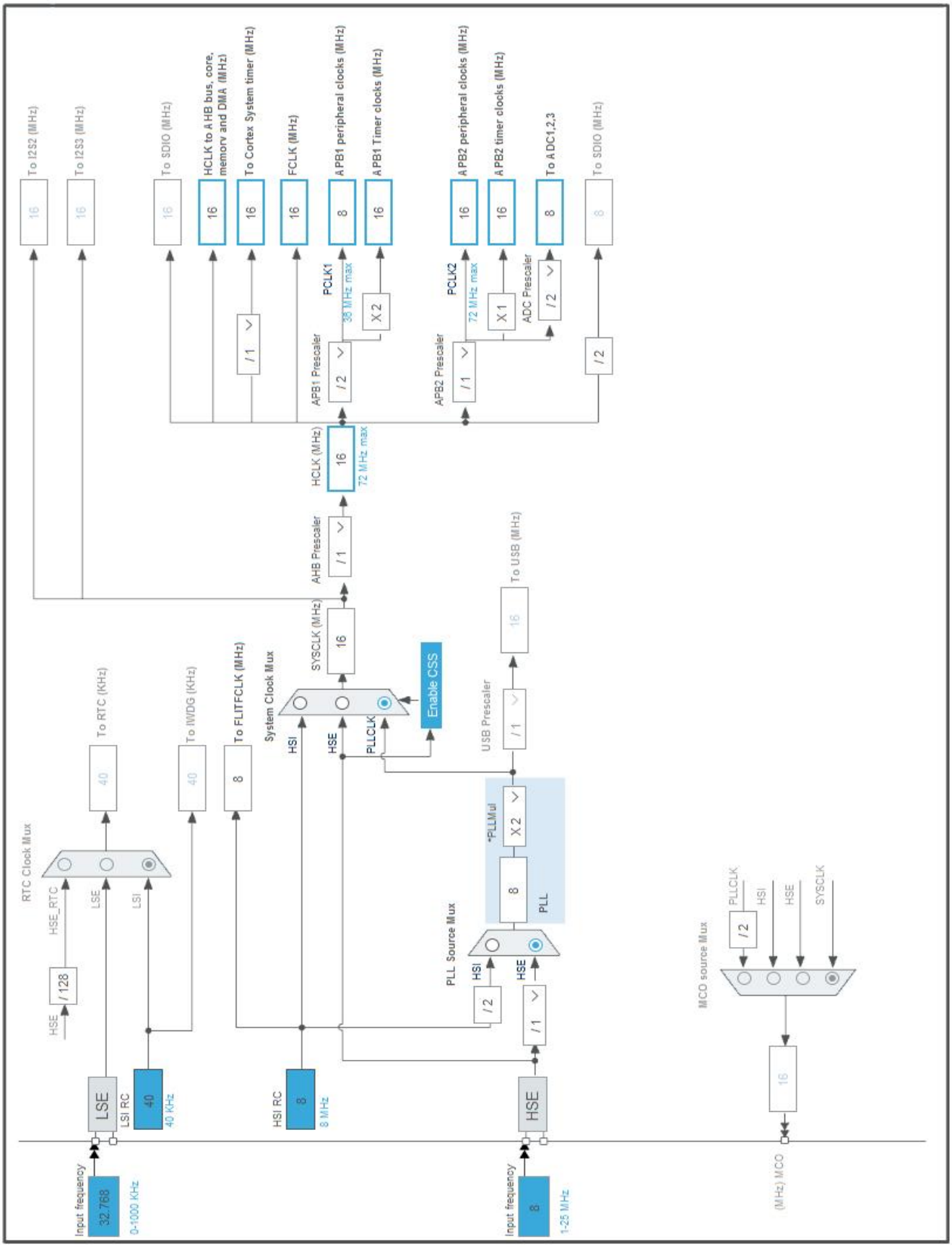
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	GPIO_Analog, ADC2_IN10	LEFT_DC_CUR_PIN
9	PC1	I/O	GPIO_Analog, ADC1_IN11	RIGHT_DC_CUR_PIN
10	PC2	I/O	GPIO_Analog, ADC1_IN12	DCLINK_PIN
11	PC3	I/O	GPIO_Analog, ADC2_IN13	LEFT_V_CUR_PIN
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	GPIO_Analog, ADC1_IN0	LEFT_U_CUR_PIN
15	PA1 *	I/O	GPIO_Input	BUTTON_PIN
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	BUZZER_PIN
21	PA5 *	I/O	GPIO_Output	OFF_PIN
23	PA7	I/O	TIM8_CH1N	LEFT_TIM_UL_PIN
24	PC4	I/O	GPIO_Analog, ADC1_IN14	
25	PC5	I/O	GPIO_Analog, ADC2_IN15	RIGHT_V_CUR_PIN
26	PB0	I/O	TIM8_CH2N	LEFT_TIM_VL_PIN
27	PB1	I/O	TIM8_CH3N	LEFT_TIM_WL_PIN
28	PB2 *	I/O	GPIO_Output	LED_PIN
29	PB10	I/O	USART3_TX	
30	PB11	I/O	USART3_RX	
31	VSS	Power		
32	VDD	Power		
34	PB13	I/O	TIM1_CH1N	RIGHT_TIM_UL_PIN
35	PB14	I/O	TIM1_CH2N	RIGHT_TIM_VL_PIN
36	PB15	I/O	TIM1_CH3N	RIGHT_TIM_WL_PIN
37	PC6	I/O	TIM8_CH1	LEFT_TIM_UH_PIN
38	PC7	I/O	TIM8_CH2	LEFT_TIM_VH_PIN
39	PC8	I/O	TIM8_CH3	LEFT_TIM_WH_PIN

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	PA8	I/O	TIM1_CH1	RIGHT_TIM_UH_PIN
42	PA9	I/O	TIM1_CH2	RIGHT_TIM_VH_PIN
43	PA10	I/O	TIM1_CH3	RIGHT_TIM_WH_PIN
45	PA12 *	I/O	GPIO_Input	CHARGER_PIN
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
51	PC10 *	I/O	GPIO_Input	
52	PC11 *	I/O	GPIO_Input	RIGHT_HALL_V_PIN
53	PC12 *	I/O	GPIO_Input	RIGHT_HALL_W_PIN
56	PB4 *	I/O	GPIO_Input	LEFT_HALL_V_PIN
57	PB5 *	I/O	GPIO_Input	LEFT_HALL_U_PIN
59	PB7 *	I/O	GPIO_Input	LEFT_HALL_W_PIN
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	SideBoardMX
Project Folder	D:\git_others\HoverboardMX
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.7.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RCTx
Datasheet	14611_Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

mode: IN11

mode: IN12

mode: IN14

mode: Temperature Sensor Channel

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**5 ***
External Trigger Conversion Source	**Timer 8 Trigger Out event ***
Rank	1
Channel	**Channel 14 ***
Sampling Time	**7.5 Cycles ***
Rank	**2 ***
Channel	Channel 0
Sampling Time	**7.5 Cycles ***
Rank	**3 ***
Channel	**Channel 11 ***
Sampling Time	**13.5 Cycles ***
Rank	**4 ***
Channel	**Channel 12 ***
Sampling Time	**13.5 Cycles ***
Rank	**5 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**239.5 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN10

mode: IN13

mode: IN15

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**3 ***
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	**Channel 15 ***
Sampling Time	**7.5 Cycles ***
Rank	**2 ***
Channel	**Channel 13 ***
Sampling Time	**7.5 Cycles ***
Rank	**3 ***
Channel	Channel 10
Sampling Time	**13.5 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : BYPASS Clock Source

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel3: PWM Generation CH3 CH3N

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 16 bits value)	**64000000 / 2 / PWM_FREQ ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Enable (CNT_EN) ***

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	**Low ***

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	**Enable ***
Off State Selection for Idle Mode (OSSI)	**Enable ***
Lock Configuration	Off
Dead Time	**DEAD_TIME ***

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	**Low ***
CH Idle State	Reset
CHN Idle State	**Set ***

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	**Low ***
CH Idle State	Reset
CHN Idle State	**Set ***

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	**Low ***
CH Idle State	Reset
CHN Idle State	**Set ***

7.6. TIM8

Slave Mode: Gated Mode

Trigger Source: ITR0

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N
Channel2: PWM Generation CH2 CH2N
Channel3: PWM Generation CH3 CH3N
7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 16 bits value)	**64000000 / 2 / PWM_FREQ ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Gated Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	**Enable (Trigger delayed for master/slaves simultaneous start) ***
Trigger Event Selection	**Update Event ***

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	**Low ***

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	**Enable ***
Off State Selection for Idle Mode (OSSI)	**Enable ***
Lock Configuration	Off
Dead Time	**DEAD_TIME ***

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	**Low ***
CH Idle State	Reset
CHN Idle State	**Set ***

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

CHN Polarity	**Low ***
CH Idle State	Reset
CHN Idle State	**Set ***

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	**Low ***
CH Idle State	Reset
CHN Idle State	**Set ***

7.7. USART2

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	**CONTROL_BAUD ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.8. USART3

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	DEBUG_BAUD
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	n/a	n/a	RIGHT_DC_CUR_PIN
	PC2	ADC1_IN12	Analog mode	n/a	n/a	DCLINK_PIN
	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	LEFT_U_CUR_PIN
	PC4	ADC1_IN14	Analog mode	n/a	n/a	
ADC2	PC0	ADC2_IN10	Analog mode	n/a	n/a	LEFT_DC_CUR_PIN
	PC3	ADC2_IN13	Analog mode	n/a	n/a	LEFT_V_CUR_PIN
	PC5	ADC2_IN15	Analog mode	n/a	n/a	RIGHT_V_CUR_PIN
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PB13	TIM1_CH1N	Alternate Function Push Pull	n/a	Low	RIGHT_TIM_UL_PIN
	PB14	TIM1_CH2N	Alternate Function Push Pull	n/a	Low	RIGHT_TIM_VL_PIN
	PB15	TIM1_CH3N	Alternate Function Push Pull	n/a	Low	RIGHT_TIM_WL_PIN
	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	RIGHT_TIM_UH_PIN
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	RIGHT_TIM_VH_PIN
	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	RIGHT_TIM_WH_PIN
TIM8	PA7	TIM8_CH1N	Alternate Function Push Pull	n/a	Low	LEFT_TIM_UL_PIN
	PB0	TIM8_CH2N	Alternate Function Push Pull	n/a	Low	LEFT_TIM_VL_PIN
	PB1	TIM8_CH3N	Alternate Function Push Pull	n/a	Low	LEFT_TIM_WL_PIN
	PC6	TIM8_CH1	Alternate Function Push Pull	n/a	Low	LEFT_TIM_UH_PIN
	PC7	TIM8_CH2	Alternate Function Push Pull	n/a	Low	LEFT_TIM_VH_PIN
	PC8	TIM8_CH3	Alternate Function Push Pull	n/a	Low	LEFT_TIM_WH_PIN
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	**High ***	
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	**High ***	
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	**n/a**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
GPIO	PC0	GPIO_Analog	Analog mode	n/a	n/a	LEFT_DC_CUR_PIN
	PC1	GPIO_Analog	Analog mode	n/a	n/a	RIGHT_DC_CUR_PIN
	PC2	GPIO_Analog	Analog mode	n/a	n/a	DCLINK_PIN
	PC3	GPIO_Analog	Analog mode	n/a	n/a	LEFT_V_CUR_PIN
	PA0-WKUP	GPIO_Analog	Analog mode	n/a	n/a	LEFT_U_CUR_PIN
	PA1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTTON_PIN
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUZZER_PIN
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OFF_PIN
	PC4	GPIO_Analog	Analog mode	n/a	n/a	
	PC5	GPIO_Analog	Analog mode	n/a	n/a	RIGHT_V_CUR_PIN
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_PIN
	PA12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CHARGER_PIN
	PC10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RIGHT_HALL_V_PIN
	PC12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RIGHT_HALL_W_PIN
	PB4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LEFT_HALL_V_PIN
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LEFT_HALL_U_PIN
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LEFT_HALL_W_PIN

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low
USART3_RX	DMA1_Channel3	Peripheral To Memory	Low
USART3_TX	DMA1_Channel2	Memory To Peripheral	Low
ADC1	DMA1_Channel1	Peripheral To Memory	Low

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Channel6 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***

Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	5	0
DMA1 channel7 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupts	unused		
TIM8 capture compare interrupt	unused		

*** User modified value**

9. Software Pack Report